fHayden Miedema and Douglas Money

CIS 451

Professor Kurmas

Homework 10: Cache (Pt. 1)

1. For each cache configuration below, fill in the corresponding table column to show whether each reference is a hit or a miss.
   1. 1MB, direct-mapped cache with 4 byte blocks.
   2. 1MB, direct-mapped cache with 8 byte blocks.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **References** | **(a)** | | **(b)** | |
| 0x00000004 | 1 | Miss | 0 | Miss |
| 0x00800018 | 6 | Miss | 3 | Miss |
| 0x00D00010 | 4 | miss | 2 | Miss |
| 0x00000004 | 1 | hit | 0 | hit |
| 0x0080001C | 7 | miss | 3 | hit |
| 0x00D00014 | 5 | miss | 2 | hit |
| 0x00A00008 | 2 | miss | 1 | miss |
| 0x00A00004 | 1 | miss | 0 | miss |
| 0x00000008 | 2 | miss | 1 | miss |
| 0x00200030 | 12 | miss | 6 | miss |
| 0x00200024 | 9 | miss | 4 | miss |
| 0x00200034 | 13 | miss | 6 | hit |
| 0x00D00034 | 13 | hit | 6 | hit |
| 0x00200030 | 12 | hit | 6 | miss |

1. There should be four rows where columns (a) and (b) differ. Explain precisely how the change in cache configuration produces the observed behavior differences.

The cache configuration changes what index bits are being read so they are different for each. The 8 byte blocks in B will get a different index bit for each reference added to the cache so on the places where they differ an index was referenced in one that had not yet been added to the cache but had been added to the other

1. For each cache configuration below, fill in the corresponding table column to show whether each reference is a hit or a miss.
   1. 1MB, direct-mapped cache with 4 byte blocks.
   2. 1MB, direct-mapped cache with 8 byte blocks.
   3. 1MB, two-way set associative cache with 8 byte blocks.
   4. 1.5MB three-way set associative cache with 8 byte blocks

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **References** | **(a)** | | **(b)** | | **(c)** | | **(d)** | |
| 0x00000018 | 6 | Miss | 3 | Miss | 3 | Miss | 3 | Miss |
| 0x00D00018 | 6 | Miss | 3 | Miss | 3 | Miss | 3 | Miss |
| 0x00A0003C | 15 | Miss | 7 | Miss | 7 | Miss | 7 | Miss |
| 0x00D00018 | 6 | Hit | 3 | Hit | 3 | Hit | 3 | Hit |
| 0x00000018 | 6 | Miss | 3 | Miss | 3 | Hit | 3 | Hit |
| 0x00500010 | 4 | Miss | 2 | Miss | 2 | Miss | 2 | Miss |
| 0x00400004 | 1 | Miss | 0 | Miss | 0 | Miss | 0 | Miss |
| 0x00A00038 | 14 | Miss | 7 | Hit | 7 | Hit | 7 | Hit |
| 0x00400000 | 0 | Miss | 0 | Hit | 0 | Hit | 0 | Hit |
| 0x00600024 | 9 | Miss | 4 | Miss | 4 | Miss | 4 | Miss |
| 0x00500014 | 5 | Miss | 2 | Hit | 2 | Hit | 2 | Hit |
| 0x00D0001C | 7 | Miss | 3 | Hit | 3 | Hit | 3 | Hit |
| 0x00E0001C | 7 | Miss | 3 | Miss | 3 | Miss | 3 | Miss |
| 0x00D0001C | 7 | Miss | 3 | Miss | 3 | Hit | 3 | Hit |
| 0x0000001C | 7 | Miss | 3 | Miss | 3 | Hit | 3 | Hit |

1. Compute the total number of bits required to implement the caches described below given a 32-bit address space. Fill in the requested information in the table provided. List (1) the total number of bits per line, (2) the total number of bytes of SRAM needed, and (3) the "overhead" as a percentage of data. (For example, a 1MB cache that requires 1.25MB of data total would have a 25% overhead.) Don't forget to include the valid bit and any LRU bits if necessary. Assume the number of LRU bits is n - 1 for an n-way set associative cache.
   1. 1MB direct-mapped cache with 1 byte blocks (Patterson and Hennessy problem 7.9)
   2. 1MB direct-mapped cache with 4 byte blocks (Patterson and Hennessy problem 7.10)
   3. 1MB 2-way set associative cache with 1 byte blocks and LRU replacement (Patterson and Hennessy problem 7.25 -- almost)
   4. 1MB 2-way set associative cache with 4 byte blocks and LRU replacement
   5. 1MB fully associative cache with 1 byte blocks and LRU replacement (Patterson and Hennessy problem 7.26)
   6. 1MB fully associative cache with 4 byte blocks and LRU replacement (Patterson and Hennessy problem 7.27)

# lines = (cache size / block size) / (associativity)

Total size = (# bits / line ) \* (# of lines)

1. 1MB direct-mapped cache with 1 byte blocks (Patterson and Hennessy problem 7.9)

|  |  |  |
| --- | --- | --- |
| Tag  12 | Index  20 | Offset  0 |

Cache Row

|  |  |  |
| --- | --- | --- |
| Valid  1 | Tag  12 | Data  8 |

1) 21 bits per line

2) 2752512 bytes of SRAM

3) 61.9% of SRAM is overhead

1. 1MB direct-mapped cache with 4 byte blocks (Patterson and Hennessy problem 7.10)

|  |  |  |
| --- | --- | --- |
| Tag  12 | Index  18 | Offset  2 |

Cache Row

|  |  |  |
| --- | --- | --- |
| Valid  1 | Tag  12 | Data  32 |

1) 45 bits per line

2) 1474560 bytes of SRAM

3) 28.8% of SRAM is overhead

1. 1MB 2-way set associative cache with 1 byte blocks and LRU replacement (Patterson and Hennessy problem 7.25 -- almost)

Instruction

|  |  |  |
| --- | --- | --- |
| Tag  13 | Index  19 | Offset  0 |

Cache Row

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Valid  1 | Tag  13 | Data  8 | Valid  1 | Tag  13 | Data  8 | LRU  1 |

1) 45 bits per line

2) 2949120 bytes of SRAM

3) 64.4% of SRAM is overhead

1. 1MB 2-way set associative cache with 4 byte blocks and LRU replacement

Instruction

|  |  |  |
| --- | --- | --- |
| Tag  13 | Index  17 | Offset  2 |

Cache Row

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Valid  1 | Tag  13 | Data  32 | Valid  1 | Tag  13 | Data  32 | LRU  1 |

1) 93 bits per line

2) 1523712 bytes of SRAM

3) 31.2% of SRAM is overhead

1. 1MB fully associative cache with 1 byte blocks and LRU replacement (Patterson and Hennessy problem 7.26)

Instruction

|  |  |  |
| --- | --- | --- |
| Tag  32 | Index  0 | Offset  0 |

Cache Row

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Valid  1 | Tag  32 | Data  8 | ... | Valid  1 | Tag  32 | Data  8 | LRU  (2^20) - 1 |

1) 22020096 bits per line

2) 2752512 bytes of SRAM

3) 61.9% of SRAM is overhead

1. 1MB fully associative cache with 4 byte blocks and LRU replacement (Patterson and Hennessy problem 7.27)

Instruction

|  |  |  |
| --- | --- | --- |
| Tag  30 | Index  0 | Offset  2 |

Cache Row

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Valid  1 | Tag  30 | Data  32 | ... | Valid  1 | Tag  30 | Data  32 | LRU  (2^18) - 1 |

1) 16777215 bits per line

2) 2097151.875 bytes of SRAM

3) 50% of SRAM is overhead